Notice of References Cited	Application/Control No. 10/010,572	Applicant(s)/Patent Under Reexamination CAVANAGH ET AL.	
	Examiner Ayal I. Sharon	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Agrawal, P. et al. "A Hardware Logic Simulation System." IEEE Transactions on CAD of Integrated Circuits and Systems. Jan. 1990. Vol. 9, Issue 1, pp.19-29.
	V	Agrawal, P. et al. "Architecture and Design of the MARS Hardware Accelerator." Proc. of the 24th ACM/IEEE Conf. on Design Automation. 1987. pp.101-107.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.